DATA SHEET

74ALVCH16823

18-bit bus-interface D-type flip-flop with reset and enable (3-State)

Product specification

1998 Jul 29

IC24 Data Handbook

Philips Semiconductors

PHILIPS

18-bit D-type flip-flop (3-State) 74ALVCH16823

FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- Multibyte™flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins to minimize noise and ground bounce
- All data inputs have bus hold
- Output drive capability 50Ω transmission lines @ 85°C

DESCRIPTION

The 74ALVCH16823 is a 18-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. Incorporates bushold data inputs which eliminate the need for external pull-up resistors to hold unused inputs. The74ALVCH16823 consists of two sections of nine edge-triggered flip-flops. A clock (CP) input, an output-enable ($\overline{OE}$) input, a Master reset ($\overline{MR}$) input and a clock-enable($\overline{CE}$) input are provided for each total 9-bit section.

With the clock-enable ($\overline{CE}$) input LOW, the D-type flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition. Taking $\overline{CE}$ HIGH disables the clock buffer, thus latching the outputs. Taking the Master reset ($\overline{MR}$) input LOW causes all the Q outputs to go LOW independently of the clock.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of flip-flops.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

QUICK REFERENCE DATA

GND = 0V; T_{amb} = 25°C; $t_r = t_f \leq 2.5$ns

SYMBOL	PARAMETER	CONDITIONS		TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay CP to Qn	V_{CC} = 2.5V, CL = 30pF V_{CC} = 3.3V, CL = 50pF		2.1 2.1	ns
F_{max}	Maximum clock frequency	V_{CC} = 2.5V, CL = 30pF V_{CC} = 3.3V, CL = 50pF		300 350	MHz
C_I	Input capacitance			5.0	pF
C_{PD}	Power dissipation capacitance per latch	V_I = GND to V_{CC}[1]	Outputs enabled	16	pF
			Outputs disabled	10	

NOTES:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz; C_L = output load capacity in pF;
   f_o = output frequency in MHz; V_{CC} = supply voltage in V;
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

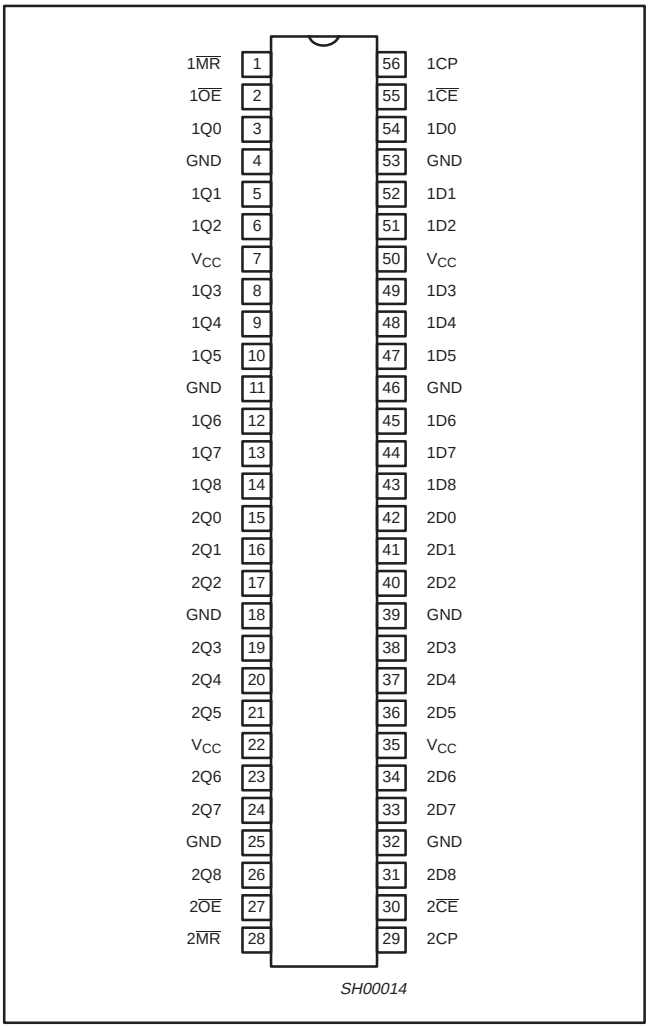
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type II	-40°C to +85°C	74ALVCH16823 DL	ACH16823 DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74ALVCH16823 DGG	ACH16823 DGG	SOT364-1

PIN DESCRIPTION

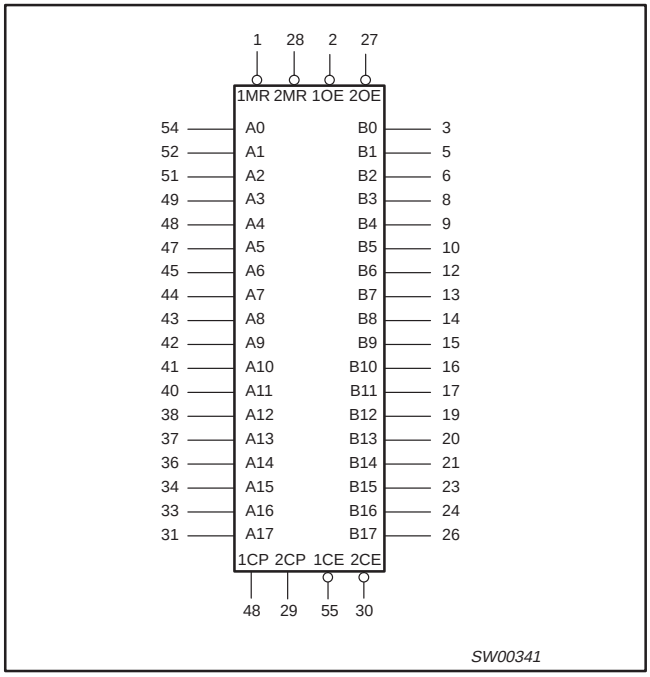
PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	1D0-1D8 2D0-2D8	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	1Q0-1Q8 2Q0-2Q8	Data outputs
56, 29	1CP, 2CP	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

PIN CONFIGURATION



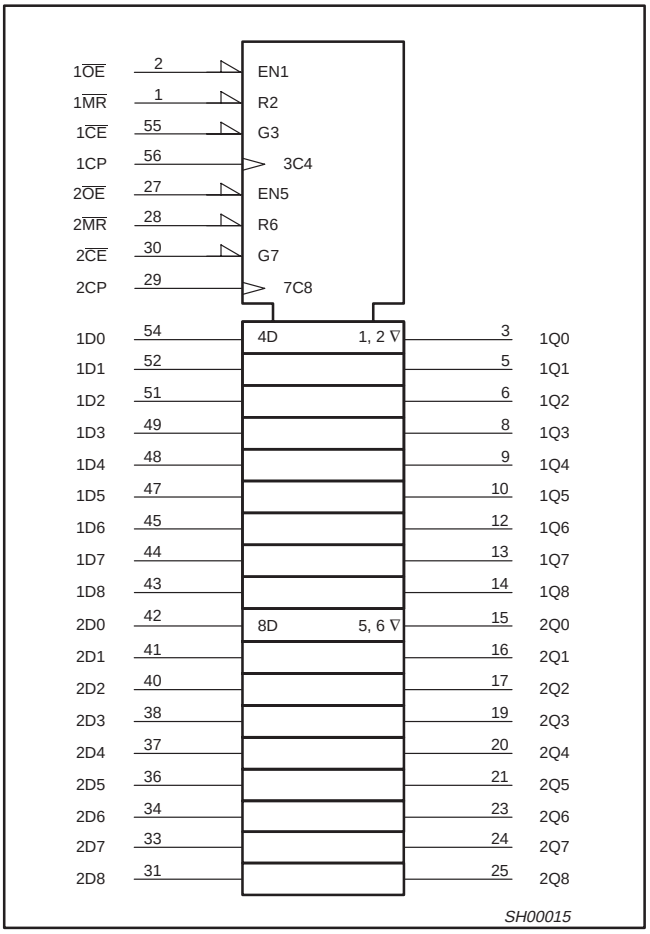
SH00014

LOGIC SYMBOL

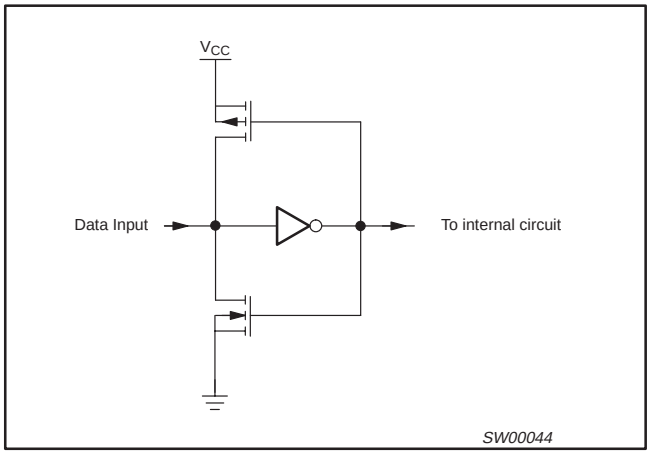


SW00341

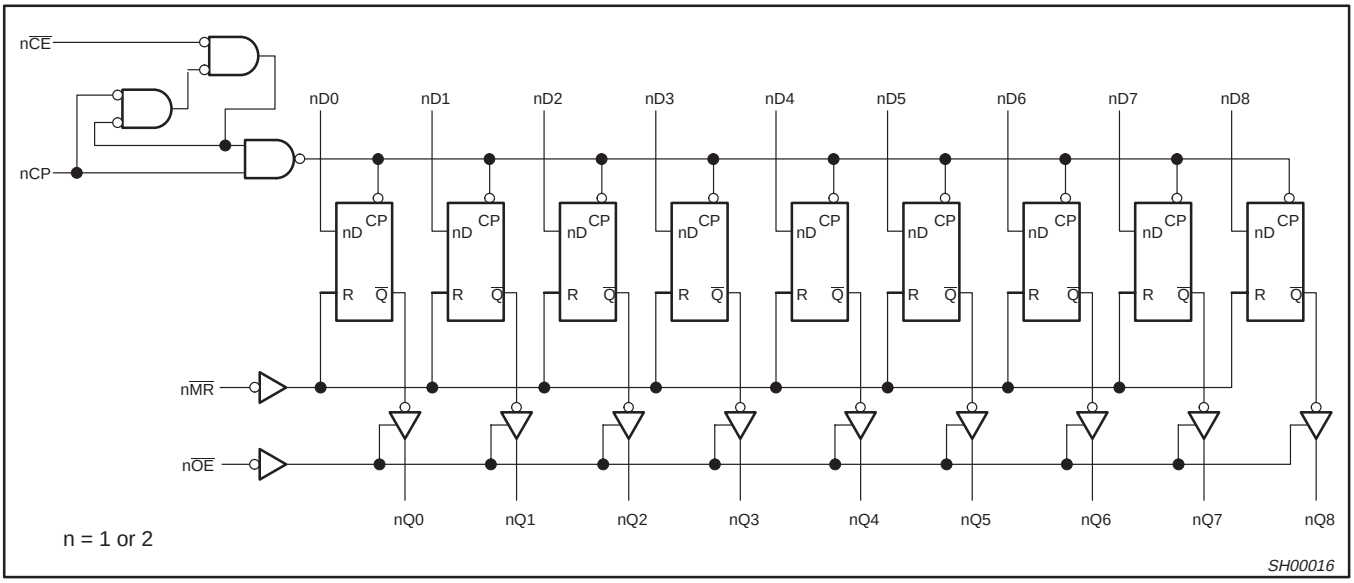
LOGIC SYMBOL (IEEE/IEC)



BUS HOLD CIRCUIT



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUT	OPERATING MODES
$n\overline{OE}$	$n\overline{MR}$	$n\overline{CE}$	nCP	nDx	nQx	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	L	L	X	Q_0	Hold
L	H	H	X	X	Q_0	
H	X	X	X	X	Z	Disable outputs

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the Low-to-High clock transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
Z = HIGH impedance "off" state
↑ = LOW to High clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load)		2.3	2.7	V
	DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load)		3.0	3.6	
V_{CC}	DC supply voltage (for low-voltage applications)		1.2	3.6	V
V_I	DC Input voltage range	for data input pins	0	V_{CC}	V
		for control pins	0	5.5	V
V_O	DC output voltage range		0	V_{CC}	V
T_{amb}	Operating free-air temperature range		–40	+85	°C
t_r, t_f	Input rise and fall times	V_{CC} = 2.3 to 3.0V V_{CC} = 3.0 to 3.6V	0 0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage	For control pins[1]	–0.5 to +5.5	V
		For data inputs[1]	–0.5 to V_{CC} +0.5	
I_{OK}	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
V_O	DC output voltage	Note 1	–0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current	V_O = 0 to V_{CC}	±50	mA
I_{GND}, I_{CC}	DC V_{CC} or GND current		±100	mA
T_{stg}	Storage temperature range		–65 to +150	°C
P_{TOT}	Power dissipation per package –plastic medium-shrink (SSOP) –plastic thin-medium-shrink (TSSOP)	For temperature range: –40 to +125 °C above +55°C derate linearly with 11.3 mW/K above +55°C derate linearly with 8 mW/K	 850 600	mW

NOTE:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP[1]	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2V	V_{CC}			V
		V_{CC} = 1.8V	0.7*V_{CC}	0.9		
		V_{CC} = 2.3 to 2.7V	1.7	1.2		
		V_{CC} = 2.7 to 3.6V	2.0	1.5		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2V		–	GND	V
		V_{CC} = 1.8V		0.9	0.2*V_{CC}	
		V_{CC} = 2.3 to 2.7V		1.2	0.7	
		V_{CC} = 2.7 to 3.6V		1.5	0.8	
V_{OH}	HIGH level output voltage	V_{CC} = 1.8 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = –100µA	V_{CC} – 0.2	V_{CC}	–	V
		V_{CC} = 1.8V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.4	V_{CC} – 0.10	–	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –6mA	V_{CC} – 0.3	V_{CC} – 0.08	–	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.17	–	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = –18mA	V_{CC} – 0.6	V_{CC} – 0.26	–	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = –12mA	V_{CC} – 0.5	V_{CC} – 0.14	–	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = –24mA	V_{CC} – 1.0	V_{CC} – 0.28	–	
V_{OL}	LOW level output voltage	V_{CC} = 1.8 to 3.6V; V_I = V_{IH} or V_{IL}; I_O = 100µA		GND	0.20	V
		V_{CC} = 1.8V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.09	0.30	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 6mA		0.07	0.20	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.15	0.40	
		V_{CC} = 2.3V; V_I = V_{IH} or V_{IL}; I_O = 18mA		0.23	0.60	
		V_{CC} = 2.7V; V_I = V_{IH} or V_{IL}; I_O = 12mA		0.14	0.40	
		V_{CC} = 3.0V; V_I = V_{IH} or V_{IL}; I_O = 24mA		0.27	0.55	
I_I	Input leakage current per control pin	V_{CC} = 1.8 to 3.6V; V_I = 5.5V or GND		0.1	5	µA
	Input leakage current per data pin	V_{CC} = 1.8 to 3.6V; V_I = V_{CC} or GND		0.1	5	
I_{IHZ}/I_{ILZ}	Input current for common I/O pins	V_{CC} = 1.8 to 2.7V; V_I = V_{CC} or GND		0.1	10	µA
		V_{CC} = 3.6V; V_I = V_{CC} or GND		0.1	15	
I_{OZ}	3-State output OFF-state current	V_{CC} = 1.8 to 2.7V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	5	µA
		V_{CC} = 2.7 to 3.6V; V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND		0.1	10	
ΔI_{CC}	Additional quiescent supply current given per data I/O pin	V_{CC} = 2.7V to 3.6V; V_I = V_{CC} – 0.6V; I_O = 0		150	750	µA
I_{BHL}	Bus hold LOW sustaining current	V_{CC} = 2.3V; V_I = 0.7V[2]	45	–		µA
		V_{CC} = 3.0V; V_I = 0.8V[2]	75	150		
I_{BHH}	Bus hold HIGH sustaining current	V_{CC} = 2.3V; V_I = 1.7V[2]	–45			µA
		V_{CC} = 3.0V; V_I = 2.0V[2]	–75	–175		
I_{BHLO}	Bus hold LOW overdrive current	V_{CC} = 2.7V[2]	300			µA
		V_{CC} = 3.6V[2]	450			
I_{BHHO}	Bus hold HIGH overdrive current	V_{CC} = 2.7V[2]	–300			µA
		V_{CC} = 3.6V[2]	–450			

NOTES:

1. All typical values are at T_{amb} = 25°C.
2. Valid for data inputs of bus hold parts.

AC CHARACTERISTICS FOR V_{CC} = 2.3V TO 2.7V RANGE AND V_{CC} < 2.3V

GND = 0V; $t_r = t_f \leq 2.0$ns; C_L = 30pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS							UNIT
			V_{CC} = 2.3 to 2.7V			V_{CC} = 1.8V			V_{CC} = 1.2V	
			MIN	TYP[1, 2]	MAX	MIN	TYP1	MAX	TYP[1]	
t_{PLH}/t_{PHL}	Propagation delay nCP to nQ_n	1, 5	1.0	2.8	4.9	1.5	4.5	7.5	10.6	ns
t_{PLH}/t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	2, 5	1.0	2.9	5.0	1.5	4.6	7.4	9.9	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.8	5.3	1.5	4.4	7.7	10.4	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.2	4.1	1.5	3.3	5.5	6.7	ns
t_W	nCP pulse width	1, 5	3.0	1.6		4.0	2.0			ns
	$n\overline{MR}$ pulse width, LOW	3, 5	3.0	0.4		4.0	0.8			
t_{SU}	Set up time nD_n to nCP	3, 5	1.2	0.2		1.5	0.2			ns
	Set up time $n\overline{CE}$ to nCP		1.8	–0.2		2.0	–0.2			
t_h	Hold time nD_n to nCP	3, 5	0.8	–0.1		0.6	–0.2			ns
	Hold time $n\overline{CE}$ to nCP		0.3	0.2		0.3	0.2			
t_{rec}	Recovery time $n\overline{MR}$ to nCP	2, 5	1.0	0.3		0.8	0.2			ns
F_{max}	Maximum clock pulse frequency	1, 5	150	300		125	250			MHz

NOTE:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 2.5V.

AC CHARACTERISTICS FOR V_{CC} = 3.0V TO 3.6V RANGE AND V_{CC} = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; C_L = 50pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			V_{CC} = 3.0 ± 0.3V			V_{CC} = 2.7V			
			MIN	TYP[1, 2]	MAX	MIN	TYP[1]	MAX	
t_{PLH}/t_{PHL}	Propagation delay nCP to nQ_n	1, 5	1.0	2.5	3.7	1.0	2.7	4.3	ns
t_{PLH}/t_{PHL}	Propagation delay $n\overline{MR}$ to nQ_n	2, 5	1.0	2.6	4.0	1.0	3.1	4.6	ns
t_{PZH}/t_{PZL}	3-State output enable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.5	4.3	1.0	3.1	5.2	ns
t_{PHZ}/t_{PLZ}	3-State output disable time $n\overline{OE}_n$ to nQ_n	4, 5	1.0	2.8	3.9	1.0	3.1	4.3	ns
t_W	nCP pulse width HIGH or LOW	1, 5	2.5	1.4		3.0	1.6		ns
	$n\overline{MR}$ pulse width HIGH or LOW	3, 5	2.5	0.3		3.0	0.6		
t_{SU}	Set up time nD_n to nCP	3, 5	1.2	0.2		1.5	0.4		ns
	Set up time $n\overline{CE}$ to nCP		1.5	–0.1		1.9	–0.1		
t_h	Hold time nD_n to nCP	3, 5	0.8	0.0		0.6	–0.2		ns
	Hold time $n\overline{CE}$ to nCP		0.5	0.1		0.4	0.1		
t_{rec}	Recovery time $n\overline{MR}$ to nCP	2, 5	1.0	0.2		0.8	0.1		ns
F_{max}	Maximum clock pulse frequency	1, 5	200	350		150	300		MHz

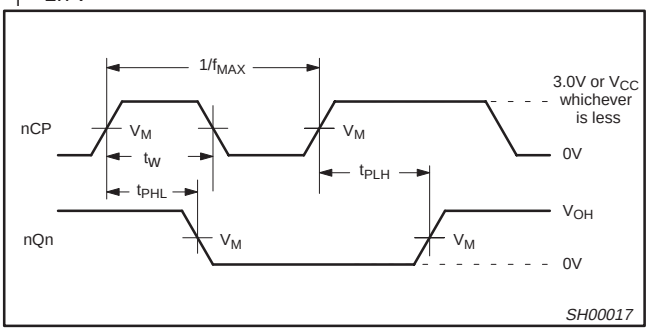
NOTES:
1. All typical values are measured at T_{amb} = 25°C.
2. Typical value is measured at V_{CC} = 3.3V.

AC WAVEFORMS FOR V_{CC} = 2.3V TO 2.7V AND V_{CC} < 2.3V RANGE

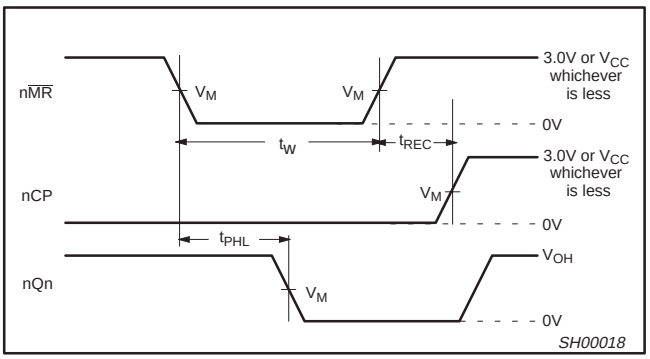
$V_M = 0.5\ V_{CC}$
$V_X = V_{OL} + 0.15V$
$V_Y = V_{OH} – 0.15V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = V_{CC}$

AC WAVEFORMS FOR V_{CC} = 3.0V TO 3.6V AND V_{CC} = 2.7V RANGE

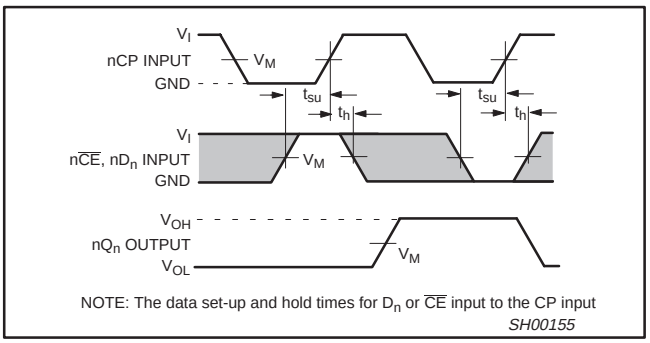
$V_M = 1.5\ V$
$V_X = V_{OL} + 0.3V$
$V_Y = V_{OH} – 0.3V$
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
$V_I = 2.7V$



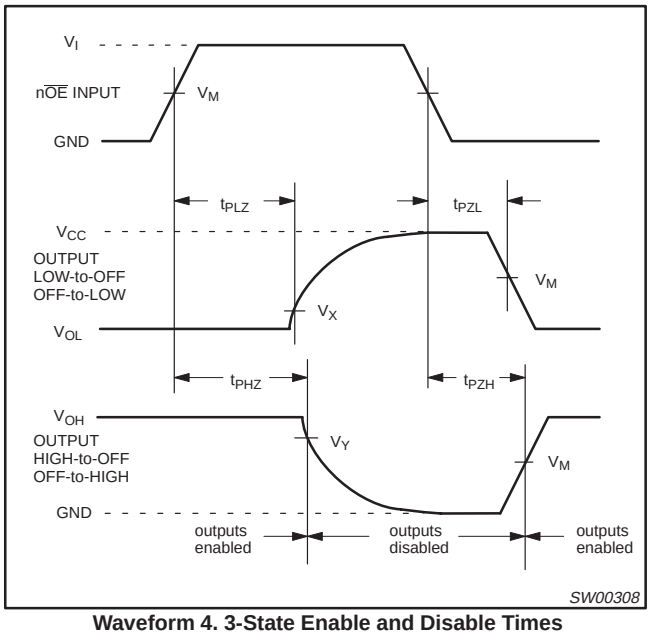
Waveform 1. Clock (nCP) to Output (nQn) Propagation Delays, Clock Pulse Width, and Maximum Clock Pulse Frequency



Waveform 2. Master Reset ($\overline{MR}$) Pulse WIdth, $\overline{MR}$ to Output propagation Delay and $\overline{MR}$ to Clock Recovery Time

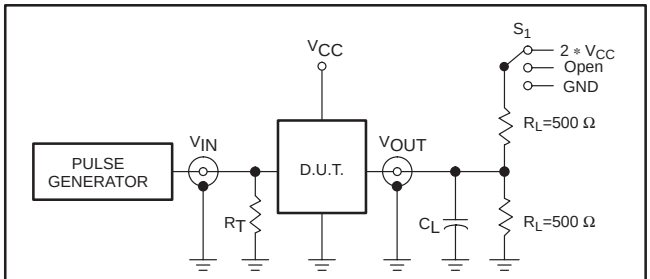


Waveform 3. Data Setup and Hold Times for the D_n or $\overline{CE}$ input to the CP input



Waveform 4. 3-State Enable and Disable Times

TEST CIRCUIT



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 * V_{CC}
t_{PHZ}/t_{PZH}	GND

V_{CC}	V_{IN}
< 2.7V	V_{CC}
2.7 – 3.6V	2.7V

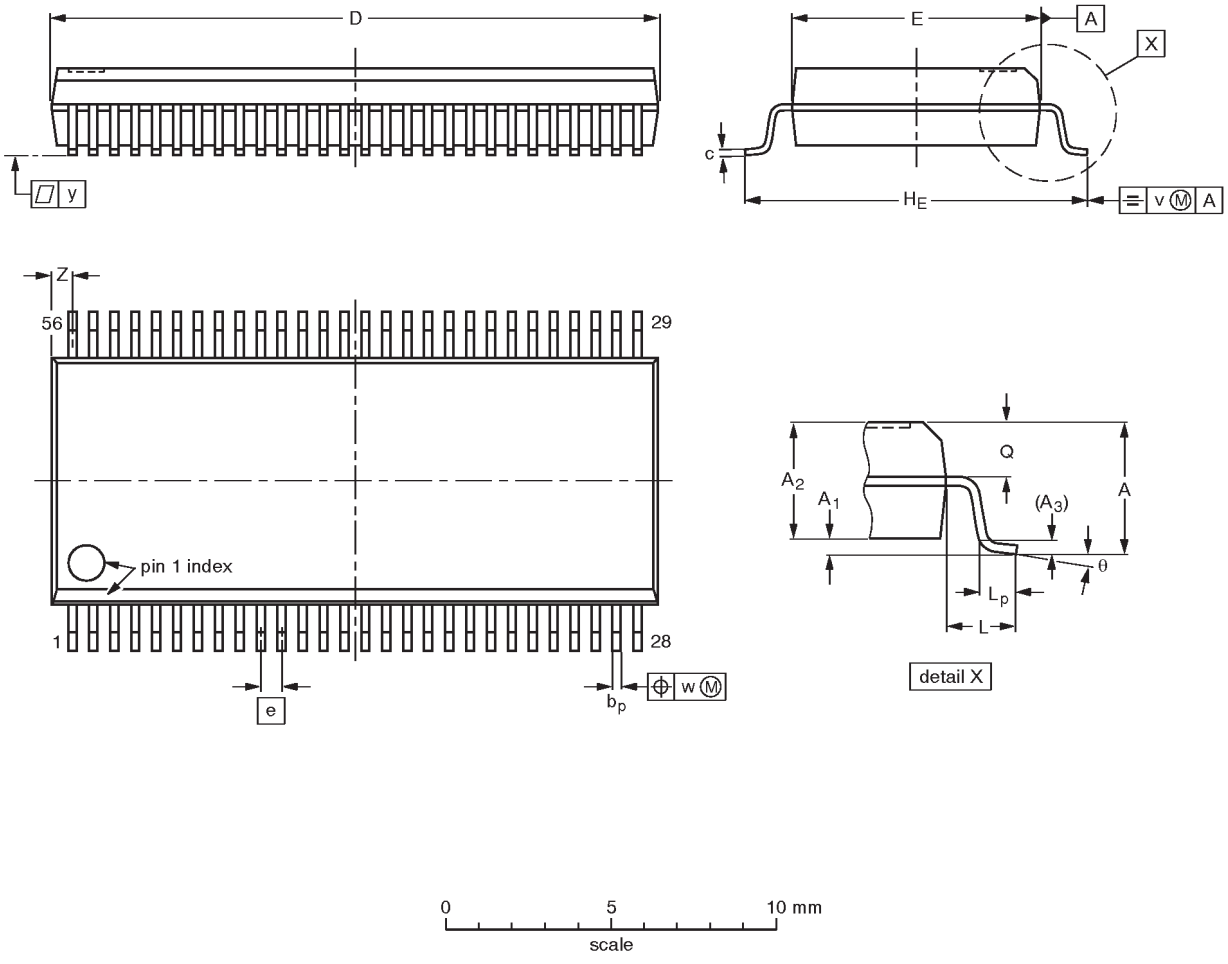
DEFINITIONS

R_L = Load resistor
C_L = Load capacitance includes jig and probe capacitance
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW00047

Waveform 5. Load circuitry for switching times

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm **SOT371-1**



DIMENSIONS (mm are the original dimensions)

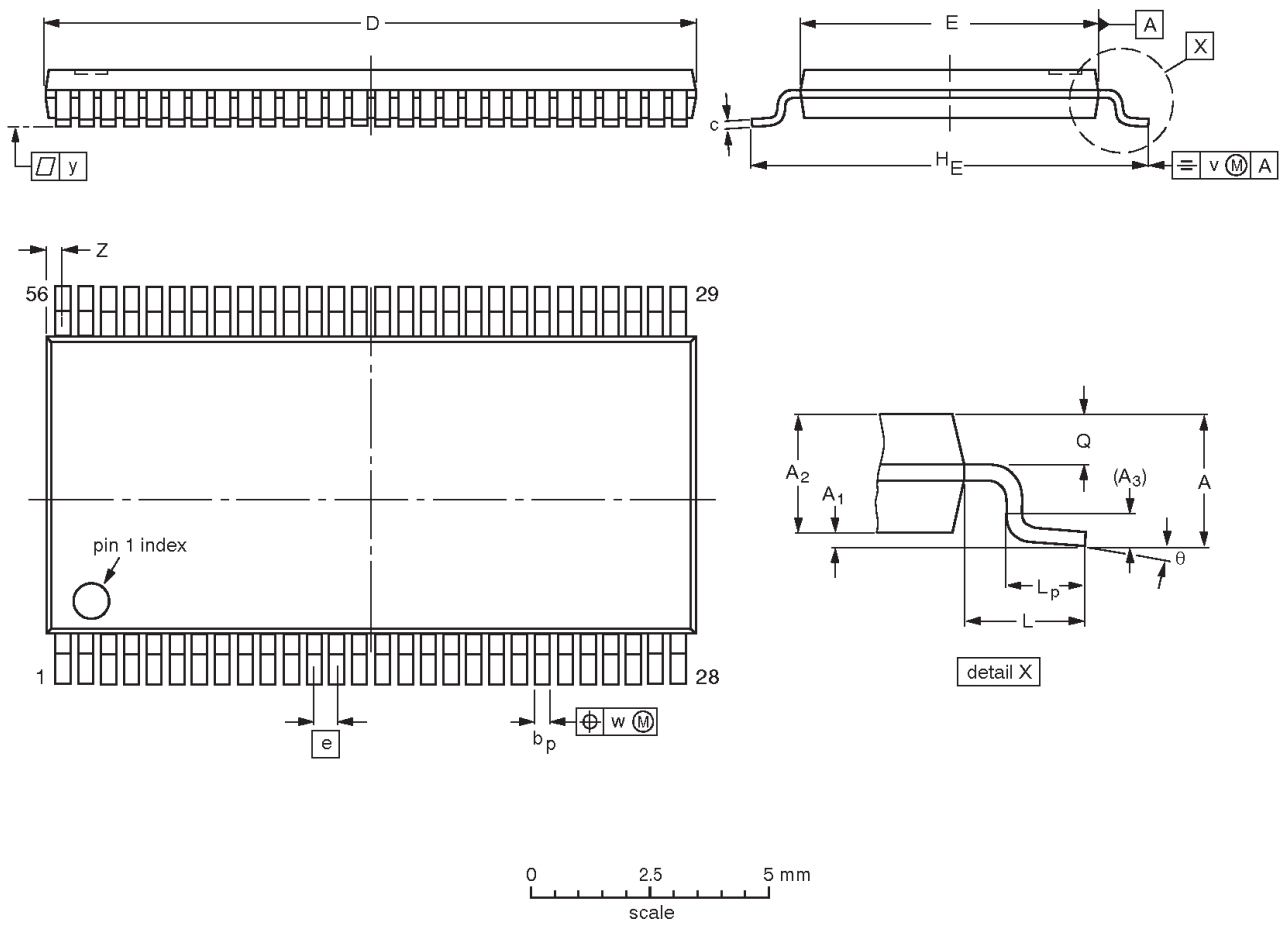
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				~~93-11-02~~ 95-02-04

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm **SOT364-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT364-1		MO-153EE					~~93-02-03~~ 95-02-10

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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